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Project Code	POWER ELECTRONICS AND POWER SYSTEM IEEE PAPERS – 2016 PROJECT TITLES WITH ABSTRACT
PEPS16NXT01	**TITLE: A Virtual RLC Damper to Stabilize DC/DC Converters Having an LC Input Filter while Improving the Filter Performance.** **ABSTRACT:** The LC filter at the input of a dc/dc converter may cause instability when the converter is controlled as a constant power load (CPL) and one of the effective solutions is to reduce the output impedance of the LC input filter with different stabilization dampers. In this letter, the impact of these dampers on the LC filter is analyzed with two-port network analysis and it is found that the existing dampers all degrade the performance of the original LC input filter to some extent. In order to overcome this drawback, an RLC damper is proposed to stabilize the whole system while improving the performance of the LC input filter. In addition, this RLC damper is also designed to achieve high robustness against the parameter variations of the LC input filter. Furthermore, in order to avoid the power loss when implementing the damper physically, a control strategy for the CPL is proposed to implement the RLC damper as a virtual RLC (VRLC) damper. The actual effectiveness of the VRLC damper and its impact on the CPL are fully evaluated via two-port network analysis as well. Finally, experimental results fro- a 100-W 48–24-V buck converter with an LC input filter are presented to demonstrate the proposed VRLC damper.
PEPS16NXT02	**TITLE: An Enhanced Single-Phase Step-Up Five-Level Inverter** **ABSTRACT:** In this letter, an enhanced step-up five-level inverter is proposed for photovoltaic systems. Compared with conventional five-level inverters, the proposed topology can realize the multilevel inversion with high step-up output voltage, simple structure, and reduced number of power switches. The operating principle of the proposed inverter has been analyzed and the output voltage expression has been derived. In addition, the comparison with existing topologies of single-phase five-level inverters is presented. Finally, experimental results

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	validate the performance of the proposed topology.
PEPS16NXT03	**TITLE: A Real-Time Variable Turn-Off Current Strategy for a PFC Converter With Voltage Spike Limitation and Efficiency Improvement** **ABSTRACT:** The voltage source driver (VSD) is widely used in a conventional gate drive circuit of the power factor correction (PFC) converter. However, the fixed drive current of the VSD circuit could not optimize the switching losses, and the turn-off voltage spike across the power switch is freewill. In this letter, a real-time variable turn-off current strategy of a power switch for the PFC converter is presented. The turn-off current can be modulated real timely with the input voltage varying periodically, and the voltage spike across power switch can be controlled under the peak value that set at the peak input voltage region. The operation principle, design considerations, and the analysis of turn-off switching losses with the proposed strategy are presented by a boost PFC converter in detail. Furthermore, a prototype of the boost PFC converter was built to verify the effectiveness of the proposed strategy. As a result, the turn-off voltage spike is well limited and the efficiency is effectively improved compared with the VSD.
PEPS16NXT04	**TITLE: Interleaved Boundary Conduction Mode Versus Continous Conduction Mode Magnetic Volume Comparison in Power Converters** **ABSTRACT:** Power converters operating in boundary conduction mode (BCM) can benefit from an efficiency increase compared to continuous conduction mode (CCM) based on the soft-switching transitions at turn-on and/or turn-off. However, for a given average inductor current, the RMS current in BCM converters becomes larger than in CCM converters, leading to an increase in conduction losses. Interleaving smaller BCM power converters overcome this drawback by reducing the total ripple current amplitude at the expense of an increase in complexity and in magnetic parts count. Nevertheless, as the magnetic devices are among the largest components in power converters, it is convenient to find the design conditions under which BCM or CCM could yield the smaller net volume. This paper proposes a method to estimate the volume

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	ratio for magnetic parts, between single-phase CCM and multiple interleaved BCM power converters as a function of the number of phases, inductor loss, and switching frequency. The results obtained can be applied to boost, forward, and flyback dc-to-dc topologies.
PEPS16NXT05	**TITLE: A Novel DBC Layout for Current Imbalance Mitigation in SiC MOSFET Multichip Power Modules** **ABSTRACT:** This letter proposes a novel direct bonded copper (DBC) layout for mitigating the current imbalance among the paralleled SiC mosfet dies in multichip power modules. Compared to the traditional layout, the proposed DBC layout significantly reduces the circuit mismatch and current coupling effect, which consequently improves the current sharing among the paralleled SiC mosfet dies in power module. Mathematic analysis and circuit model of the DBC layout are presented to elaborate the superior features of the proposed DBC layout. Simulation and experimental results further verify the theoretical analysis and current balancing performance of the proposed DBC layout.
PEPS16NXT06	**TITLE: Enhanced Frequency-Locked Loop With a Comb Filter Under Adverse Grid Conditions** **ABSTRACT:** To improve the performance of frequency-locked loops (FLLs) under distorted grid conditions, the technique of harmonic decoupling with multiple notch filters was usually employed to remove the harmonic components, which, although offering good filtering abilities, suffers from complexity, high computational burden, and deteriorated dynamics. To alleviate these problems, this letter proposes an enhanced adaptive notch-filter-based FLL, which incorporates a comb filter and improves the filtering abilities by introducing purely imaginary zeros to achieve notch peaks and harmonic cancellation. In comparison with the typical existing solutions of multiple notch-filter-based FLLs for distorted grid systems, the proposed FLL features simple structure and low computational load, and it can completely block the dc component, odd and even harmonics of the input grid voltage without sacrificing the FLL dynamics.

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	Experimental results and comparisons are presented to validate the effectiveness of the proposed FLL.
PEPS16NXT07	**TITLE: Modeling the Output Impedance of a T-Type Power Converter** **ABSTRACT:** The impact of operating point dependent switching time delays on the output characteristic of a T-type half-bridge is investigated for dc–dc operation. It is found that a series connection of operating point dependent components, i.e., a differential resistance and a voltage source, can accurately reproduce the implications of these switching time delays on the response of the output current of the half-bridge to a step of the duty cycle. This letter details the calculation of these components and verifies the derived expressions by means of experimental results.
PEPS16NXT08	**TITLE: Failure Modes of 15-kV SiC SGTO Thyristors During Repetitive Extreme Pulsed Overcurrent Conditions** **ABSTRACT:** SiC SGTO thyristors are an advanced solution for increasing the power density of medium voltage power electronics. However, for these devices to replace Si thyristor technology in industrial applications their characteristics and failure modes must be understood. This letter presents the failure modes of two 15-kV SiC SGTO thyristors during repetitive overcurrent conditions. The devices were evaluated with 2-kA (3.85 kA/cm^2) square pulses of 100 s duration using a pulse forming network. Throughout testing, each devices' static characteristics were analyzed for signs of degradation; upon degradation, testing was ceased and the physical failure mode was determined through imaging with a scanning electron microscope (SEM) in conjunction with a focused ion beam. The electrical results demonstrate the failure modes of both SiC SGTO thyristors during pulsed overcurrents electrically manifested themselves as a conductive path through the gate-anode junction and an increased device on-state voltage. SEM imaging revealed one SiC thyristor formed an approximately wide cylindrical void, and the second SiC thyristor formed an approximately long crack. However, the experimental results demonstrate these 15-kV SiC SGTO thyristors' robust ability to repetitively switch at extreme high current density for tens of thousands

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	of cycles.
PEPS16NXT09	**TITLE: ZVS of Power MOSFETs Revisited** **ABSTRACT:** Aiming for converters with high efficiency and high power density demands converter topologies with zero-voltage switching (ZVS) capabilities. This letter shows that in order to determine whether ZVS is provided at a given operating point, the stored charge within the mosfets has to be considered and the condition has to be fulfilled. In the case of incomplete soft switching, nonzero losses occur which are analytically derived and experimentally verified in this letter. Furthermore, the issue of nonideal soft-switching behavior of Si superjunction mosfets is addressed.
PEPS16NXT10	**TITLE: An Improved Second-Order Generalized Integrator Based Quadrature Signal Generator** **ABSTRACT:** The second-order generalized integrator based quadrature signal generator (SOGI-QSG) is able to produce in-quadrature signals for many applications, such as frequency estimation, grid synchronization, and harmonic extraction. However, the SOGI-QSG is sensitive to input dc and harmonic components with unknown frequencies (e.g., interharmonics). To overcome the drawback, this letter begins by analyzing the dynamic response of SOGI-QSG from the first-order system (FOS) perspective. A second-order SOGI-QSG (SO-SOGI-QSG) with a fourth-order transfer function is then proposed, after referring to the relationship between standard FOS and second-order system. The proposed method is subsequently found to inherit the simplicity of the SOGI-QSG, while demonstrates better disturbance attenuation. Its parameter design procedure is also easy to understand, and can be followed step-by-step without difficulty. Performance of the proposed SO-SOGI-QSG is finally validated by experimental results presented in this letter.

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PEPS16NXT11	**TITLE: An Adaptive Current Injection Scheme for Resonant Capacitor ofLLC Resonant Converters With Suppressed Frequency Variation** **ABSTRACT:** LLC techniques have been popular solutions for high density power converters due to the benefits of soft switching and no reverse recovery losses. But the need of switching frequency control for output voltage regulation is always a considerable challenge for practical design. This letter proposes a simple and low-cost scheme to suppress the frequency variation for LLC resonant converters with wide range operation. An auxiliary circuit, which only deals with a relatively lower current, is utilized to regulate the output voltage by providing an adaptive current injection for the resonant capacitor. Then, by taking the benefit of controllable current injection, adjustment of the energy transferring time for the power transformer is achievable without the need of switching frequency variation, and soft switching of the power switches is still maintained. In addition to detailed theoretical analysis, experimental results verify the feasibility and effectiveness of the proposed concept.
PEPS16NXT12	**TITLE: A-Source Impedance Network** **ABSTRACT:** A novel A-source impedance network is proposed in this letter. The A-source impedance network uses an autotransformer for realizing converters for any application that demand a very high dc voltage gain. The network utilizes a minimal turns ratio compared to other magnetically coupled impedance source networks to attain a high voltage gain. In addition, the proposed converter draws a continuous current from the source, and hence it is suitable for many types of renewable energy sources. The derived network expressions and theoretical analysis are finally validated experimentally with an example single-switch 400-W dc–dc converter. For the closed-loop control design and stability assessment, a small signal model and its analysis of the proposed network are also presented in brief.

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PEPS16NXT13	**TITLE: Improved Adaptive-Series-Virtual-Impedance Control Incorporating Minimum Ripple Point Tracking for Load Converters in DC Systems** **ABSTRACT**: The adaptive-series-virtual-impedance (ASVI) control strategy is an attractive load stabilization method for cascaded systems thanks to its adaptive capacity for different source converters and better load performance. However, as reported in the previous literature, this ASVI control strategy has a potential problem: Since it utilizes a proportional-integral (PI) controller to find the center frequency of the ASVI, the PI controller may miss it with excessive proportional or integral coefficients and lead to the failure of the ASVI control strategy. Although this potential problem may not arise with small proportional and integral coefficients, it is a hidden trouble for the ASVI control strategy. To make the ASVI control strategy more reliable, a minimum-ripple-point-tracking (MRPT) controller is proposed to replace the original PI controller in this letter. With the MRPT controller, the center frequency of ASVI is found via the perturb and observe algorithm, which ensure the ASVI control strategy do not have the aforementioned potential problem anymore. Furthermore, in order to find the center frequency of ASVI quickly, the sinusoidal-tracking algorithm is further introduced into the MRPT controller to improve its processing speed. Finally, a load converter cascaded with different input filters are fabricated to validate the proposed MRPT controller.
PEPS16NXT14	**TITLE: Inductive Charger for Electric Vehicle: Advanced Modeling and Interoperability Analysis** **ABSTRACT:** This paper focuses on the interoperability analysis of a resonating contactless charging system for electric vehicles (EVs). The design uses different inductive loops realized by industrial partners. It highlights an advanced electromagnetic modeling (EM) concerning the geometrical characteristics, the resonant topologies, and the control loop. It is shown that the EV chassis plays a major role in the calculation of the electrical parameters and the radiation of the interoperable system. Furthermore, the position of the interoperable magnetic

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	couplers with respect to the EV (middle or backend) has an important effect on the values of the coupling factor and also for the radiation of the system. Finally, an efficiency of 90% is realized in the experimental test with the interoperability which gives flexibility for the driver to use charging stations with different technologies.
PEPS16NXT15	**TITLE: A Three-Phase Bidirectional AC/DC Converter With Y–Δ Connected Transformers** **ABSTRACT:** This paper proposes a three-phase bidirectional ac/dc converter with Y–Δ connected transformers. The converter achieves both buck-boost ac/dc bidirectional conversion and electrical isolation with the single-stage structure. By introducing three dc–dc transformers, the total power is distributed and the current stress of the rectifier stage decreases. The Y–Δ connected transformers provide extra step-down conversion ratio and facilitate the converters' application in buck conversion. The circuit derivation, operation principles, and control strategy with the SVPWM algorithm are presented. A 3-kW prototype with 380-V dc and a 1.6-kW prototype with 48-V dc were built in the lab and experimental results verify the theoretical analysis well.
PEPS16NXT16	**TITLE: A 50-kVA Three-Phase Solid-State Transformer Based on the Minimal Topology: Dyna-C** **ABSTRACT:** The Dynamic Current or Dyna-C is a minimal topology for implementing the bidirectional three-phase solid-state transformer (SST). While only two current-source power conversion stages are employed, the Dyna-C SST has features of voltage step up/down, arbitrary power factors, and frequencies between the input and output terminals. In this paper, a compact 50-kVA three-phase SST based on this minimal topology is designed. More specifically, design considerations and practical implementation techniques are presented. Results from experimental measurements are shown and discussed.

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PEPS16NXT17	**TITLE: Design and Development of a Class EF Inverter and Rectifier for Multimegahertz Wireless Power Transfer Systems** **ABSTRACT:** This paper presents the design and implementation of a Class EF inverter and Class EF rectifier for two -W wireless power transfer (WPT) systems, oneoperating at 6.78 MHz and the other at 27.12 MHz. It will be shown that the Class EF circuits can be designed to have beneficial features for WPT applications such as reduced second-harmonic component and lower total harmonic distortion, higher power-output capability, reduction in magnetic core requirements and operation at higher frequencies in rectification compared to other circuit topologies. A model will first be presented to analyze the circuits and to derive values of its components to achieve optimum switching operation. Additional analysis regarding harmonic content, magnetic core requirements and open-circuit protection will also be performed. The design and implementation process of the two Class-EF -based WPT systems will be discussed and compared to an equivalent Class-E-based WPT system. Experimental results will be provided to confirm validity of the analysis. A dc–dc efficiency of 75% was achieved with Class-EF -based systems.
PEPS16NXT18	**TITLE: Space-Vector PWM With Common-Mode Voltage Elimination for Multiphase Drives** **ABSTRACT:** Switching common-mode voltage (CMV) generated by the pulse width modulation (PWM) of the inverter causes common-mode currents, which lead to motor bearing failures and electromagnetic interference problems in multiphase drives. Such switching CMV can be reduced by taking advantage of the switching states of multilevel multiphase inverters that produce zero CMV. Specific space-vector PWM (SVPWM) techniques with CMV elimination, which only use zero CMV states, have been proposed for three-level five-phase drives, and for open-end winding five-, six-, and seven-phase drives, but such methods cannot be extended to a higher number of levels or phases. This paper presents a general (for any number of levels and phases) SVPMW with CMV elimination. The

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	proposed technique can be applied to most multilevel topologies, has low computational complexity and is suitable for low-cost hardware implementations. The new algorithm is implemented in a low-cost field-programmable gate array and it is successfully tested in the laboratory using a five-level five-phase motor drive.
PEPS16NXT19	**TITLE: A Novel Multiple-Frequency Resonant Inverter for Induction Heating Applications** **ABSTRACT:** This paper presents a novel multiple-frequency resonant inverter for induction heating (IH) applications. By adopting a center tap transformer, the proposed resonant inverter can give load switching frequency as twice as the isolated-gate bipolar transistor (IGBT) switching frequency. The structure and the operation of the proposed topology are described in order to demonstrate how the output frequency of the proposed resonant inverter is as twice as the switching frequency of IGBTs. In addition to this, the IGBTs in the proposed topology work in zero-voltage switching during turn-on phase of the switches. The new topology is verified by the experimental results using a prototype for IH applications. Moreover, increased efficiency of the proposed inverter is verified by comparison with conventional designs.
PEPS16NXT20	**TITLE: Tolerance Band Adaptation Method for Dynamic Operation of Grid-Connected Modular Multilevel Converters** **ABSTRACT:** The use of modular multilevel converters (MMC) in high-voltage direct current (HVdc) transmission systems has grown significantly in the past decade. The efficiency, cell capacitor voltage ripple, and dynamic performance are three contradictory aspects of the MMC which are related to the converter switching scheme. Previously introduced tolerance band (TB)-based schemes enable efficient and simple control for grid-connected MMCs. This paper addresses the dynamic operation of TB switching schemes by proposing a dynamic boundary setting technique for steady-state operation and a switching scheme scheduling controller for transient fault handling. The performance of

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	proposed methods are validated in a realistic point-to-point HVdc link, modeled in real-time digital simulator where two converters with 512 cells per arm are implemented. Utilizing the proposed methods will enable efficient implementation of TB-based schemes for different operating points, and also a robust transient fault handling.
PEPS16NXT21	**TITLE: Analysis and Control of M3C-Based UPQC for Power Quality Improvement in Medium/High-Voltage Power Grid** **ABSTRACT:** To enhance the power quality in the medium/high-voltage distribution power systems, a single-phase unified power quality conditioner (UPQC) based on the modular multilevel matrix converter (M3C) is presented in this paper. The M3C-UPQC is comprised of four identical multilevel converter arms and associated filtering inductors. According to the established equivalent circuit of M3C-UPQC, its operation principle and power balance of each arm are analyzed theoretically, and the parameters' design for the arm inductance as well as submodule capacitance is studied. Then, an integrated control method for M3C-UPQC in which the dc circulating current is used to balance the instantaneous active power of each arm is proposed to prevent the capacitor voltages from divergence inter- and intra-arms, so as to achieve voltages balance of M3C-UPQC. Finally, the effectiveness of the proposed control method is verified by a prototype rated at 8 kVA.
PEPS16NXT22	**TITLE: Assessment of the Current-Source, Full-Bridge Inverter as Power Supply for Ozone Generators With High Power Factor in a Single Stage** **ABSTRACT:** The arrangement of the full-bridge, current-source inverter as a power supply for ozone generators providing high power factor (PF) and high electrical efficiency in a single stage is the main contribution of this paper. The corresponding design, simulation, and experimental results are presented. Also, the use of the current-fed, full-bridge resonant inverter for PF correction in ozone generation applications is discussed. The proposed power supply consists of an ac supply, a single rectifier bridge, an input inductor to the inverter, four switches,

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	an LC parallel resonant tank, a resonant transformer, and a set of ozone generating cells. Experimental results with the proposed topology provided 96% for PF, 91% for electrical efficiency, and ozone production of 614 mgO_3/min, satisfying the requirements of the standard 61000-3-2, class A.
PEPS16NXT23	**TITLE: Leakage Current Calculation for PV Inverter System Based on a Parasitic Capacitor Model** **ABSTRACT:** The occurrence of leakage current that can occur in photovoltaic (PV) system depends strongly on the value of parasitic capacitance between PV panel and the ground. However, traditional method to acquire that value is by experience estimation. This paper presents a novel 2-D parasitic edge capacitance model and a straightforward approach to accurately calculate the involved panel parasitic capacitance. The parasitic capacitances are divided into cell-to-frame capacitance , cell-to-rack capacitance , and cell-to-ground capacitance . Based upon that, a pi-shape circuit model is derived to predict the leakage current in the PV array. Theoretical calculation, MATLAB simulations, and experimental measurements finally verify the accuracy of the proposed methods. The approaches are very useful for the evaluation of leakage current in the PV system. It is demonstrated that the proposed approach combines the ease of applications and satisfying accurateness.
PEPS16NXT24	**TITLE: Single-Stage Three-Phase Differential-Mode Buck-Boost Inverters With Continuous Input Current for PV Applications** **ABSTRACT:** Differential-mode buck-boost inverters have merits such as reduced switch number, ability to provide voltages higher or lower than the input voltage magnitude, improved efficiency, reduced cost and size, and increased power density, especially in low-power applications. There are five buck-boost inverters that can provide flexible output voltage without the need of a large electrolytic input side capacitor, which degrades the reliability of inverters. The continuous input current of these inverters is appropriate for maximum power point tracking operation in photovoltaic and fuel cells applications. Three of the five inverters

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	can be isolated with high-frequency-link transformers where the common-mode leakage current can be mitigated. However, the performance and control of such converters have not been discussed in detail. In this paper, the five possible single-stage three-phase differential-mode buck-boost inverters with continuous input current are investigated and compared in terms of total losses, maximum ripple current, total harmonic distortion, and device and passive element ratings. In addition, the possible methods are presented for eliminating the input third-order harmonic current, resulting from the stored energy in the passive elements, as well as the output second-order harmonic currents. The ability for isolating the input and output sides of the inverters with a small–high frequency transformers is discussed. A changeable-terminal 2.5-kW bidirectional inverter is used to validate the design flexibility of the inverter topologies, when digital signal processor-controlled.
PEPS16NXT25	**TITLE: Energy Compression of Dielectric Barrier Discharge With Third Harmonic Circulating Current in Current-Fed Parallel-Series Resonant Converter** **ABSTRACT:** An advanced technique of energy compression with the third harmonic circulating current generation is presented in this paper to improve the surface treatment performance in the dielectric barrier discharge (DBD) systems. First, the relationship between the energy compression degree and contact angle is explored, which shows that the polymer surface wettability can be improved by the high energy compression degree in DBD. And then, an additional inductor is inserted into the resonant tank in the current-fed parallel-series resonant converter to generate the third harmonic current component, which can reduce the discharge-time-ratio and compress the energy transferred to the DBD loads. Furthermore, the method of rectifier-compensated fundamental plus third harmonic approximation (RCFTHA) is introduced to describe the current-fed parallel-series resonant converter by superposing two equivalent linear circuits operating at the fundamental and third harmonic frequencies, respectively. Consequently, the discharge-time-ratio optimization with the parallel-series resonant tank design is realized. Finally, the experimental results from a 350-W

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	prototype substantiate the effectiveness of the energy compression with the third harmonic circulating current and the accuracy of RCFTHA.
PEPS16NXT26	**TITLE: Multidimensional Space-Vector PWM Algorithm Using Branch Space Voltage Vector** **ABSTRACT:** Typical algorithms of multidimensional space-vector pulsewidth modulation (SVPWM) divide (n –1) dimensional space into (n–1)/2 subplanes with decoupling matrix or symmetrical component approach. However, the determination of effective sectors and appropriate space voltage vectors takes a heavy computing burden. Taking the five-phase inverter as example, the relationship between the operation time of branch switches and the dwell times of active space vectors in the SVPWM method is analyzed in this paper. Then, the branch space voltage vector (BSVV) corresponding to the individual active branch voltage is defined and the synthesis of other active space voltage vectors using BSVVs is given. Furthermore, only the BSVVs are chosen as the base vectors to synthesize the reference voltage vector, and a novel SVPWM algorithm is present. The operation time of branch switch is deduced, and the equivalence of the normalized load-phase voltages and operation times of branch switches is emphasized and used to analyze the simulation results. The zero-sequence voltage vector is also included in the algorithm as a parameter and its effects on the dwell time of the BSVVs, the modulation index and the common-mode voltage are explicated. Finally, the extension to an n-phase system is discussed. The algorithm eliminates the selection of sectors and proper active space vectors, and can effectively control the dwell time of switches of multiphase inverter. Experimental results proved the feasibility and effectiveness of the algorithm.

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PEPS16NXT27	**TITLE: Digital Control of a High-Voltage (2.5 kV) Bidirectional DC--DC Flyback Converter for Driving a Capacitive Incremental Actuator** **ABSTRACT:** This paper presents a digital control technique to achieve valley switching in a bidirectional flyback converter used to drive a dielectric electroactive polymer-based capacitive incremental actuator. This paper also provides the design of a low input voltage (24 V) and variable high output voltage (0–2.5 kV) bidirectional dc–dc flyback converter for driving a capacitive incremental actuator. The incremental actuator consists of three electrically isolated mechanically connected capacitive actuators. It requires three high-voltage (HV) (2–2.5 kV) bidirectional dc–dc converters to accomplish the incremental motion by charging and discharging the capacitive actuators. The bidirectional flyback converter employs a digital controller to improve the efficiency and charge/discharge speed using the valley switching technique during both charge and discharge processes, without the need to sense signals on the output HV side. Experimental results verifying the bidirectional operation of a HV flyback converter are presented using a 3-kV polypropylene-film capacitor as the load. The energy-loss distributions of the converter are presented when 4- and 4.5-kV HV mosfets are used on HV side. The flyback prototype with a 4 kV mosfet demonstrated 89% charge energy efficiency to charge the capacitive load from 0 V to 2.5 kV, and 84% discharge energy efficiency to discharge it from 2.5 kV to 0 V.
PEPS16NXT28	**TITLE: Simplified Space Vector Modulation Techniques for Multilevel Inverters** **ABSTRACT:** This paper presents simplified techniques for the space vector modulation (SVM) of any n-level multilevel inverter. Three techniques have been presented to simplify the identification of the nearest three vectors to the reference vector. The first two techniques are based on resolving the multilevel inverter space vector diagram into appropriate two-level hexagons. This results in simplification of the multilevel SVM problem into a two-level SVM problem. The third technique is an algorithm-based technique which makes use of a 60°-

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	spaced gh coordinate system to perform the SVM of a multilevel inverter. Switching sequence design for all the three techniques is presented with the aim of minimization of the device switching frequency. Simulation and experimental results have been provided to verify the feasibility of the proposed techniques. Simulation results are provided for up to 21-level cascaded H-bridge (CHB) inverters, while the experimental verification is done on a five-level laboratory prototype. Although only the CHB inverter is considered in this study, the proposed techniques are perfectly general and can be applied to all types of multilevel inverters, and are extendable to any number of levels.
PEPS16NXT29	**Title: An Inductive and Capacitive Combined Wireless Power Transfer System With LC-Compensated Topology** **ABSTRACT:** This paper proposes a combined inductive and capacitive wireless power transfer (WPT) system with LC -compensated topology for electric vehicle charging application. The circuit topology is a combination of the LCC-compensated inductive power transfer (IPT) system and the LCLC-compensated capacitive power transfer (CPT) system. The working principle of the combined circuit topology is analyzed in detail, providing the relationship between the circuit parameters and the system power. The design of the inductive and capacitive coupling is implemented by the finite-element analysis. The equivalent circuit model of the coupling plates is derived. A 3.0-kW WPT system is designed and implemented as an example of combined inductive and capacitive coupling. The inductive coupler size is 300 mm × 300 mm and the capacitive coupler is 610 mm × 610 mm. The air-gap distance is 150 mm for both couplers. The output power of the combined system is the sum of the IPT and CPT system. The prototype has achieved 2.84-kW output power with 94.5% efficiency at 1-MHz switching frequency, and performs better under misalignment than the IPT System. This demonstrates that the inductive–capacitive combined WPT system is a potential solution to the electric vehicle charging application.

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PEPS16NXT30	**TITLE: Unified Digital Current Mode Control Tuning With Near Optimal Recovery in a CCM Buck Converter** **ABSTRACT:** Linear small-signal models of a dc–dc converter often ignore switching dynamics; thus such models are insufficient to fully explore the performance objective under large signal transients. Linear/nonlinear hybrid controllers are promising alternatives; however, they require structurally different hardware resources along with extra antiwindup arrangements. This paper proposes a geometric tuning method in a digitally current-mode-controlled buck converter under continuous-conduction mode. This considers a proportional-integral voltage controller along with a load current feedforward in the digital domain, while the inductor current has a traditional analog implementation. This resembles a first-order switching surface with near load-invariant regulation; thus a (fixed) small integral gain is sufficient to minimize the steady-state error. Using phase-plane geometry, the objective is to tune the controller gain in a way to achieve proximate time optimal recovery using a fixed-frequency pulse-width modulator and also to retain the large-signal stability. The effects of parameter variation and finite sampling are analyzed. The proposed tuning is implemented using an FPGA device.
PEPS16NXT31	**TITLE: Moment-Based Discontinuous Phasor Transform and its Application to the Steady-State Analysis of Inverters and Wireless Power Transfer Systems** **ABSTRACT:** Power electronic devices are inherently discontinuous systems. Square waves, produced by interconnected transistors, are commonly used to control inverters. This paper proposes a novel phasor transform, based on the theory of moments, which allows to analyze the steady-state behavior of discontinuous power electronic devices in closed-form, i.e., without approximations. In the first part of this paper, it is shown that the phasors of an electric circuit are the moments on the imaginary axis of the linear system describing the circuit. Exploiting this observation, in the second part of this paper, we focus on the analysis of circuits powered by discontinuous sources. The new “discontinuous phasor transform” is defined and the characteristics for inductors,

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	capacitors, and resistors are described in terms of this new phasor transform. Since the new quantities maintain their physical meaning, the instantaneous power and average power can be computed in the phasor domain. The analytic potential of the new tool is illustrated studying the steady-state response of power inverters and of wireless power transfer systems with non-ideal switches.
PEPS16NXT32	**TITLE: A -Converter That Reduces Common Mode Currents, Output Voltage Ripples, and Total Capacitance Required** **ABSTRACT:** In this paper, a single-phase converter consisting of two legs with four switches, called the -converter, is proposed. It has a common ac and dc ground, which reduces common mode currents and removes the need for an isolation transformer, and two capacitors: one across the whole dc bus and the other across the output. The dc bus capacitor provides a direct path for the double-frequency ripple current inherently existing in single-phase converters to returncontinuously so the output capacitor can be sized very small, only to filter out switching ripples. Moreover, the dc bus capacitor is intentionally designed to store the system ripple energy with large voltage ripples, which reduces its capacitance. Hence, the total capacitance needed and the output voltage ripples are reduced at the same time. This makes it cost-effective to use highly reliable film capacitors instead of bulky and vulnerable electrolytic capacitors. Because of the removed isolation transformers and bulky electrolytic capacitors, the power density and system reliability are improved. In order to properly operate the converter, two independent controllers are designed for the two legs, respectively, to achieve the desired functions and other normal objectives, such as the unity power factor. Experimental results are presented to demonstrate the high performance of the proposed converter.
PEPS16NXT33	**TITLE: Interleaved Current Control for Multiphase Converters With High Dynamics Mean Current Tracking** **ABSTRACT:** This paper presents a current control for high-power multiphase converters, where fast and precise current reference tracking is required, and

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	limited switching frequency is present. The proposed control is based on a synchronization signal and current error comparison bands per phase. The control calculates the switching time that adjusts the phase current error zero-crossing points with the synchronization signal to control the current mean value and provide the correct phase shift among phases. The aforementioned comparison bands allow us to determine the current error slopes required to calculate the switching instants. This methodology permits the precise current reference tracking regardless the load voltage and the voltage drop in the semiconductor devices and in the series resistance of the phase inductors. Additionally, band-crossing information allows the fast detection of major changes in the current error, and the optimal system behavior decision, minimizing the transient time. Furthermore, the current control is stable in the complete duty cycle range, which is evaluated by means of a small-signal model. Experimental tests on a low-scale four-phase buck converter validate the proposal.
PEPS16NXT34	**TITLE: A Gate Driver With Integrated Deadtime Controller** **ABSTRACT:** Deadtimes are required to avoid simultaneous conduction of high-side and low-side power transistors in half-bridge power converters. During these secure times, free-wheeling current flow generates extra power losses. Very short deadtimes are desired but they cannot be safely set in conventional isolated power converters because of a digital input propagation delay mismatch. A specific deadtime management is introduced in this paper to ensure proper operation of a high-voltage synchronous power converter. A controller integrated in each isolated gate driver secures synchronous switching by detecting the opposite switch turn-off before turn-on. With such a selfswitching technique, very short but safe nonoverlap times can be set. A gate driver has been implemented in a 0.35 µm 20-V CMOS process. The monolithically integrated controller consumes only 140 µA and 0.22 mm^2 of silicon area. The proposed local deadtime management has been validated in two synchronous buck converters without external free-wheeling diodes: a 500-W 250-V to 55-V

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	converter based on SiC JFETs and a 30-W 45-V to 10-V converter based on eGaN FETs. In either case, the proposed controller allows a higher efficiency from 10% of the rated load with resulting deadtimes as short as 15 ns.
PEPS16NXT35	**TITLE: Improved Control Strategy of a Supercapacitor-Based Energy Recovery System for Elevator Applications** **ABSTRACT:** This paper proposes an improved control strategy for a supercapacitor (SC)-based energy recovery system (ERS) for elevator applications. The ERS is connected to the dc-link of the elevator motor drive through a bidirectional dc–dc converter for storing and then recovering the braking energy. A system of two fuzzy-logic controllers is introduced for online adjusting the dc-link voltage through the dc–dc converter of the ERS, according to the elevator operating conditions and the ac-grid voltage variations. Thus, the reduction in the consumed energy by the grid in an elevator operating cycle and, therefore, increase in the elevator system efficiency is achieved. Also, the developed control system keeps the SCs current ripple low in order to protect the SCs from overheating and, therefore, preserves their energy storage capability and operating lifetime. The proposed control scheme can be easily installed without requiring modifications to the elevator motor drive and, thus, it can be applied to any elevator system, even existing elevator installations. The effectiveness and the resulting operational improvements of the proposed control scheme have been experimentally validated on a real elevator system.
PEPS16NXT36	**TITLE: Combined Phase-Shift and Frequency Modulation of a Dual-Active-Bridge AC–DC Converter With PFC** **ABSTRACT:** This paper presents a combined phase-shift and frequency modulation scheme of a dual–active-bridge (DAB) ac–dc converter with power factor correction (PFC) to achieve zero voltage switching (ZVS) over the full range of the ac mains voltage. The DAB consists of a half bridge with bidirectional switches on the ac side and a full bridge on the dc side of the isolation transformer to accomplish single-stage power conversion. The modulation

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	scheme is described by means of analytical formulas, which are used in an optimization procedure to determine the optimal control variables for minimum switch commutation currents. Furthermore, an ac current controller suitable for the proposed modulation scheme is described. A loss model and measurements on a 3.3-kW electric vehicle battery charger to connect to the 230 / 50-Hz mains considering a battery voltage range of 280–420 V validate the theoretical analysis.
PEPS16NXT37	**TITLE: Advanced Accelerated Power Cycling Test for Reliability Investigation of Power Device Modules** **ABSTRACT:** This paper presents an apparatus and methodology for an advanced accelerated power cycling test of insulated-gate bipolar transistor (IGBT) modules. In this test, the accelerated power cycling test can be performed under more realistic electrical operating conditions with online wear-out monitoring of tested power IGBT module. The various realistic electrical operating conditions close to real three-phase converter applications can be achieved by the simple control method. Further, by the proposed concept of applying the temperature stress, it is possible to apply various magnitudes of temperature swing in a short cycle period and to change the temperature cycle period easily. Thanks to a short temperature cycle period, test results can be obtained in a reasonable test time. A detailed explanation of apparatus such as configuration and control methods for the different functions of accelerated power cycling test setup is given. Then, an improved in situ junction temperature estimation method using on-state collector–emitter voltage and load current is proposed. In addition, a procedure of advanced accelerated power cycling test and test results with 600 V, 30 A transfer molded IGBT modules are presented in order to verify the validity and effectiveness of the proposed apparatus and methodology. Finally, physics-of-failure analysis of tested IGBT modules is provided.

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PEPS16NXT38	**TITLE: Nonisolated Two-Channel LED Driver With Automatic Current Balance and Zero-Voltage Switching** **ABSTRACT:** In this paper, a nonisolated two-channel light-emitting diode (LED) driver with automatic current balance and zero-voltage switching (ZVS) is presented. In this LED driver, a dc-blocking capacitor is connected with one side of the coupled inductor. Therefore, based on the ampere–second balance, a current source is generated with the average value of the positive current identical to the absolute average value of the negative current. Accordingly, the LED currents can be balanced naturally without extra active components or current sharing transformer. Consequently, the circuit components can keep at a low count. In addition, the proposed LED driver can achieve ZVS turn-on. Thus, the switching loss can be decreased. Above all, the proposed two-channel LED driver can be extended to a multichannel LED driver. In this paper, detailed theoretical analyses and experimental results are provided to verify the feasibility and effectiveness of the proposed LED driver.
PEPS16NXT39	**TITLE: A General Design Method of Primary Compensation Network for Dynamic WPT System Maintaining Stable Transmission Power** **ABSTRACT**: Dynamic wireless power transmission (DWPT) is considered as a solution to the problems encountered in the development of electrical vehicle (EV), such as range anxiety resulted from battery bottleneck and the difficulty of convenient charging. However, the requirement of DWPT, maintaining almost constant transmission power with constant voltage load in effective movement process, is quite different from Stationary WPT. The power fluctuation is easily brought by the coupling coils over large misalignment in movement. A general design method of primary compensation network from the perspective of DWPT is presented in this paper. Under the premise of ensuring high transmission efficiency and soft switching, a novel T-type compensation network for DWPT is proposed, which maintains a stable output characteristic over a wide misalignment, companied with an inherent current limiting ability under no-load operation. A WPT prototype with a fixed frequency operation based on the T-

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	type compensation network is built. The output power is kept almost stable even though magnetic coupling coefficient varies twice showing the effectiveness of the design method.
PEPS16NXT40	**TITLE: Dual-Space Vector Control of Open-End Winding Permanent Magnet Synchronous Motor Drive Fed by Dual Inverter** **ABSTRACT:** This paper proposes a dual-space vector control scheme for the open-end winding permanent magnet synchronous motor (OEW-PMSM) drive fed by the dual inverter with a single dc supply. Potential zero-sequence current in the open-end winding drive system has to be considered since it causes circulating current in the winding and leads to high current stress of power semiconductor devices and high losses. Zero-sequence current in open-end winding ac motor drives is usually caused by the zero-sequence voltage, and therefore switching combinations which do not produce zero-sequence voltage are used to synthesize the reference voltage in existing methods. But even so, the zero-sequence voltage can also be produced by the dead time of the inverter. In order to suppress zero-sequence current in the OEW-PMSM drive, a dual-space vector control scheme is proposed and a novel dual-inverter space vector pulse width modulation (PWM) with the zero-sequence voltage reference is employed to regulate system zero-sequence voltage in this paper. Compared with existing dual inverter PWM strategies, the novel algorithm build a regulation mechanism for the zero-sequence voltage. The proposed method is compared with the conventional vector control by simulations and experiments, and the results shown that the proposed scheme can suppress zero-sequence current effectively.

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PEPS16NXT41	**TITLE: A 10-MHz Isolated Synchronous Class-Φ_2 Resonant Converter** **ABSTRACT:** Because of the forward recovery, the performance of the diodes degrades seriously at multimegahertz, causing extremely high power loss. So, the synchronous rectification (SR) is strongly desired in the multimegahertz resonant converters. This paper proposes a self-driven level-shifted resonant gate driver (RGD) for the SR FET in a 10-MHz isolated class-Φ_2 resonant converter. The proposed RGD provides precise switching timing for the SR so that the body diode conduction loss can be minimized. A control stage is introduced to the proposed RGD to block the circulating current and the low-impedance path in the driver to realize ON–OFF control of the converter with high efficiency. The proposed RGD also generates a tunable dc bias to increase the peak gate voltage and extend the conduction time with the optimal so that the average and the associated conduction loss can be reduced significantly. A 10-MHz prototype with 18-V input and 5-V/2-A output was built. At full load of 2 A, the proposed RGD improves the efficiency from 80.2% using the conventional RGD to 82% (an improvement of 1.8%). Compared to the efficiency of 77.3% using the diode rectification, the efficiency improvement is 4.7% at full load.
PEPS16NXT42	**TITLE: A High-Efficiency Current-Mode Buck Converter With a Power-Loss-Aware Switch-On-Demand Modulation Technique for Multifunction SoCs** **ABSTRACT:** Modern multifunction systems on chip often require a high-efficiency buck converter over a wide load current range as the main power source, for which complex multimode operation with mode detection/change is a frequent compromise between efficiency and transient response. This paper proposes a novel power-loss-aware switch-on-demand modulation (PLASOM) technique based on accurate power loss modeling to switch critical components/parameters of power loss on demand: the ON/OFF status and the size of the power transistor, the dead time, and the ON/OFF status of power-hungry subcircuits. The proposed PLASOM-based converter can work as either an adaptive on-time mechanism with constant frequency or a cycle-extended

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	adaptive ON/OFF-time mechanism with variable frequency without mode detection/change, so that the conversion efficiency and transient response can be improved. A proposed buck converter with the PLASOM technique was implemented using the TSMC 90-nm 1/3.3-V CMOS process. Experimental results show that a conversion efficiency higher than 90% was achieved over the 1–500 mA load current range, whereas the voltage variation/recovery time during the 0.1–500 mA load transient were less than 50 mV/25 µs. Performance evaluations indicate that the proposed PLASOM technique is favorable for wide load current range buck converters in terms of conversion efficiency, transient response, and voltage ripples.
PEPS16NXT43	**TITLE: All-Digital Low-Dropout Regulator With Adaptive Control and Reduced Dynamic Stability for Digital Load Circuits** **ABSTRACT:** Digitally implementable LDOs embedded within digital functional units augment their analog counterparts for ultrafine-grained power management in digital ICs. Digital load circuits represent load currents with large and infrequent current transients and require a wide voltage range of operation, preferably down to the threshold voltage ( ) of the transistor. This paper presents a discrete-time, fully digital, scan-programmable LDO macro in a low-power 0.13-µm technology operating down to 1.07×, the transistor , and featuring greater than 90% current efficiency across a 50× current range through fine-grained clock gating and adaptive control. An 8× improvement in transient response time to large load steps is achieved through switched mode control. Both transient and steady-state operation models and measurements of the LDO are presented.

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PEPS16NXT44	**TITLE: Envelope Modulator for 1.5-W 10-MHz LTE PA Without AC Coupling Capacitor Achieving 86.5% Peak Efficiency** **ABSTRACT:** An envelope modulator (EM) is presented to increase the efficiency of an RF power amplifier. In order to supply an output voltage higher than the input voltage while providing low-frequency power in the EM, a single-inductor dual-output (SIDO) converter is introduced. By employing the SIDO converter, the EM does not require an additional boost converter. In addition, a high-frequency converter (HFC) with a wide-bandwidth capability is also proposed. These two converters, the SIDO converter and the HFC, are combined in parallel without an ac coupling capacitor by employing a low-frequency current-balancing technique. The chip is implemented in a 0.18-µm CMOS process and achieves 86.5% peak efficiency while tracking a 10-MHz long-term evolution envelope signal.
PEPS16NXT45	**TITLE: Adapted NSPWM for Single DC-Link Dual-Inverter Fed Open-End Motor With Negligible Low-Order Harmonics and Efficiency Enhancement** **ABSTRACT:** In this paper, the near-state pulsewidth modulation (NSPWM), adapted to be implemented in dual-voltage-source inverter (VSI) fed open-end motor, is proposed with the aim of mitigating low-order harmonics (which lead to current total harmonic distortion (THD) minimization). The following two proposed methods are studied in detail: 1) fixing phase angle displacement (PAD) between two VSIs to 120° while adjusting the modulation index (MI); and 2) fixing MI to the predetermined value (wherein low-order harmonics are highly mitigated) while adjusting PAD. Furthermore, the proposed approaches enhance efficiency by limiting the number of commutations within the switching interval. The paper also presents the mathematical approaches to accurately determine low-order harmonic components and switching losses for dual-VSI structure. The experimental setup, including dual-VSI and open-end induction motor, is assembled in the laboratory to evaluate performance of the proposed method. Finally, the simulation results, carried out in the MATLAB/Simulink environment, are found to be in close agreement with experimental data.

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PEPS16NXT46	**TITLE: A Module-Integrated Distributed Battery Energy Storage and Management System** **ABSTRACT:** This paper introduces a module-integrated distributed battery energy storage and management system without the need for additional battery equalizers and centralized converter interface. This is achieved by integrating power electronics onto battery cells as an integrated module. Compared with the conventional centralized battery system, the modular design brings several advantages such as reduced power rating and voltage stress of power electronics, no extra equalizers or centralized converters, active thermal distribution control ability, enhanced safety and reliability, etc. The battery system can now be built by simply attaching integrated modules together. The integrated module is implemented by a synchronous bidirectional dc/dc converter with digital control techniques. The design considerations and control strategy of the system are discussed. A prototype is built that the power electronics are integrated onto the battery cell. Experimental results of a three-module system verified that the module-integrated distributed system provides satisfied functional performance without extra equalizers, centralized charger, or bidirectional dc/dc converter.
PEPS16NXT47	**TITLE: Common-Mode Voltage Reduction for Matrix Converters Using All Valid Switch States** **ABSTRACT:** This paper presents a new space vector modulation (SVM) strategy for matrix converters to reduce the common-mode voltage (CMV). The reduction is achieved by using the switch states that connect each input phase to a different output phase, or the switch state that connects all the output phases to the input phase with minimum absolute voltage. These two types of states always produce lower peak CMV than the others, especially the former ones that result in zero CMV at the output side of matrix converters. In comparison with the existing SVM methods, this strategy has a very similar software overhead and calculation time. Simulation and experiment results are shown to validate the effectiveness of the proposed modulation method in reducing not only the peak

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	value but also the root-mean-square value of the CMV.
PEPS16NXT48	**TITLE: A Family of Quasi-Switched-Capacitor Circuit-Based Dual-Input DC/DC Converters for Photovoltaic Systems Integrated With Battery Energy Storage** **ABSTRACT:** In this paper, a family of bidirectional dual-input dc/dc converters is proposed to combine a photovoltaic system and battery energy storage system. This family of converters utilizes a full-bridge, or half-bridge current-source circuit, as the primary side, and a quasi-switched-capacitor circuit as the secondary side. Depending on the power level of the primary side and voltage level of the battery, different topologies can be selected. Compared to other bidirectional multiple-input dc/dc converters with galvanic isolation, this family of converters requires less switches and passive components, reduces voltage stress on switches, and realizes soft switching for all switches. The operation principle of the converter is presented, and a power sharing strategy between two input sources is proposed. A 2-kW full-bridge circuit prototype is built in the lab, based on Gallium Nitride (GaN) switching devices. Simulation and experimental results are also presented to verify the theoretical analysis
PEPS16NXT49	**TITLE: A Four-Plate Compact Capacitive Coupler Design and LCL-Compensated Topology for Capacitive Power Transfer in Electric Vehicle Charging Application** **ABSTRACT:** This paper proposes a four-plate compact capacitive coupler and its circuit model for large air-gap distance capacitive power transfer (CPT). The four plates are arranged vertically, instead of horizontally, to save space in the electric vehicle charging application. The two plates that are on the same side are placed close to each other to maintain a large coupling capacitance, and they are of different sizes to maintain the coupling between the primary and secondary sides. The circuit model of the coupler is presented, considering all six coupling capacitors. The LCL compensation topology is used to resonate with the coupler and provide high voltage on the plates to transfer high power. The circuit model of the coupler is simplified to design the parameters of the compensation circuit. Finite-element analysis is employed to simulate the coupling capacitance and

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	design the dimensions of the coupler. The circuit performance is simulated in LTspice to design the specific parameter values. A prototype of the CPT system was designed and constructed with the proposed vertical plate structure. The prototype achieved an efficiency of 85.87% at 1.88-kW output power with a 150-mm air-gap distance.
PEPS16NXT50	**TITLE: A Low-Voltage Ride-Through Technique for Grid-Connected Converters With Reduced Power Transistors Stress** **ABSTRACT:** With more and more distributed energy resources being installed in the utility grid, grid operators start imposing the low-voltage ride-through requirement on such systems to remain grid-connected and inject reactive and/or active current to support grid voltage during fault conditions. This paper proposes a positive and negative sequence current injection method to meet such requirement. In the meantime, the proposed method can reduce the second harmonic ripples in the dc link of the power converter without violating the peak current constraint of the power transistors. The long-term reliability of the converter system can thus be improved.

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