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Project Code	VLSI IEEE PAPERS – 2016 PROJECT TITLES WITH ABSTRACT
VLSI16NXT01	**TITLE: High-Speed Hardware Implementation of Fixed and Runtime Variable Window Length 1-D Median Filters.** **ABSTRACT:** Nonlinear digital filters play an important role in digital signal processing applications. In this brief, a novel architecture is proposed for the hardware implementation of fixed and runtime variable window length one-dimensional median filters. In the proposed architecture, the maximum working clock frequency is almost independent of the median filter window length, whereas the hardware complexity is proportional to the number of samples in the window. This feature enables the construction of filters with relatively large window lengths with negligible reduction in the maximum clock frequency, whereas in previous architectures, the maximum clock frequency significantly drops as the window length is increased. The benchmark results show the efficiency of the proposed architecture in comparison with state-of-the-art techniques.
VLSI16NXT02	**TITLE: A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications** **ABSTRACT:** Transpose form finite-impulse response (FIR) filters are inherently pipelined and support multiple constant multiplications (MCM) technique that results in significant saving of computation. However, transpose form configuration does not directly support the block processing unlike direct-form configuration. In this paper, we explore the possibility of realization of block FIR filter in transpose form configuration for area-delay efficient realization of large order FIR filters for both fixed and reconfigurableapplications. Based on a detailed computational analysis of transpose form configuration of FIR filter, we have derived a flow graph for transpose form block FIR filter with optimized register complexity. A generalized block formulation is presented for transpose form FIR filter. We have derived a general multiplier-based architecture for the proposed transpose form

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	block filter for reconfigurable applications. A low-complexity design using the MCM scheme is also presented for the block implementation of fixedFIR filters. The proposed structure involves significantly less area-delay product (ADP) and less energy per sample (EPS) than the existing block implementation of direct-form structure for medium or large filter lengths, while for the short-length filters, the block implementation of direct-form FIR structure has less ADP and less EPS than the proposed structure. Application-specific integrated circuit synthesis result shows that the proposed structure for block size 4 and filter length 64 involves 42% less ADP and 40% less EPS than the best available FIR filter structure proposed for reconfigurableapplications. For the same filter length and the same block size, the proposed structure involves 13% less ADP and 12.8% less EPS than that of the existing direct-form block FIR structure.
VLSI16NXT03	**TITLE: A Low-Cost Low-Power Ring Oscillator-Based Truly Random Number Generator for Encryption on Smart Cards** **ABSTRACT:** The design of a low-cost low-power ring oscillator-based truly random number generator (TRNG) macrocell, which is suitable to be integrated in smart cards, is presented. The oscillator sampling technique is exploited, and a tetrahedral oscillator with large jitter has been employed to realize the TRNG. Techniques to improve the statistical quality of the ring oscillatorbased TRNGs' bit sequences have been presented and verified by simulation and measurement. A postdigital processor is added to further enhance the randomness of the output bits. Fabricated in the HHNEC 0.13-µm standard CMOS process, the proposed TRNG has an area as low as 0.005 mm^2. Powered by a single 1.8-V supply voltage, the TRNG has a power consumption of 40 µW. The bit rate of the TRNG after postprocessing is 100 kb/s. The proposed TRNG has been made into an IP and successfully applied in an SD card forencryption application. The proposed TRNG has passed the National Institute of Standards and Technology tests and Diehard tests.

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VLSI16NXT04	**TITLE: EMDBAM: A Low-Power Dual Bit Associative Memory With Match Error and Mask Control** **ABSTRACT:** A ternary content addressable memory (TCAM) speeds up the search process in the memory by searching through prestored contents rather than addresses. The additional don't care (X) state makes the TCAM suitable for many network applications but the large amount of cell requirement for storage consumes high power and takes a large design area. This paper presents a novel architecture of TCAM, which prestores 2 bits of data in an up-down manner and provides multiple masking operations through a single control multimasking circuit. The proposed dual bit associative memory with matcherror and mask control (EMDBAM) consumes low power and selects the valid value on matchline through match error controller. The proposed design has been implemented using a standard 45-nm CMOS technology, and the extracted layout has been simulated using SPECTRE with the supply voltage at 1 V. The proposed EMDBAM can reduce the cell area by 39% compared with a basic TCAM design with a reduction of 9.6% in the energy-delay product.
VLSI16NXT05	**TITLE: A Method to Design Single Error Correction Codes With Fast Decoding for a Subset of Critical Bits** **ABSTRACT:** Single error correction (SEC) codes are widely used to protect data stored in memories and registers. In some applications, such as networking, a few control bits are added to the data to facilitate their processing. For example, flags to mark the start or the end of a packet are widely used. Therefore, it is important to have SEC codes that protect both the data and the associated control bits. It is attractive for these codes to provide fast decoding of the control bits, as these are used to determine the processing of the data and are commonly on the critical timing path. In this brief, a method to extend SEC codes to support a few additional control bits is presented. The derived codes support fastdecoding of the additional control bits. and are

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	therefore suitable for networking applications.
VLSI16NXT06	**TITLE: A Mixed-Decimation MDF Architecture for Radix- Parallel FFT** **ABSTRACT:** This paper presents a mixed-decimation multipath delay feedback (M2 DF) approach for the radix-2^kfast Fourier transform. We employ the principle of folding transformation to derive the proposedarchitecture, which activates the idle period of arithmetic modules in multipath delay feedback (MDF)architectures by integrating the decimation-in-time operations into the decimation-in-frequency-operated computing units. Furthermore, we compare the proposed design with other efficient schemes, namely, the MDF and the multipath delay commutator (MDC) scheme theoretically and experimentally. Relying on the obtained expressions and statistics, it can be concluded that the M2DF design serves as an efficient alternative to the MDF scheme, since it achieves improved efficiency in the utilization of arithmetic resources without deteriorating the superiorities of feedback structures. In addition, the recommended design performs better in memory requirement and computing delay compared with the MDC approach.
VLSI16NXT07	**TITLE: A Performance Degradation Tolerable Cache Design by Exploiting Memory Hierarchies** **ABSTRACT:** Performance degradation tolerance (PDT) has been shown to be able to effectively improve the yield, reliability, and lifetime of an electronic product. The focus of PDT is on the particular performancedegrading faults (pdef) that only incur some performance degradation of a system without inducing any computation errors. The basic idea is that as long as the defective chips containing only the pdef can provide acceptable performance for some applications, they may still be marketable. Critical issues of PDT to be addressed include the portion of the pdef in a faulty chip and their induced performancedegradation. For a typical cache design, most of the possible faults are not pdef. In this brief, we propose a cache redesign method, called PDT cache, where all functional faults in the data-storage cells of

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	a cache (major part of the cache) can be transformed into pdef. By transforming this large number of faults into pdef, a faulty cache becomes much more likely to be still marketable. The proposed design exploits the existing hardware resources and the inherent error resilience scheme to reduce the incurred hardware overhead. The logic synthesis results show that the incurred hardware overhead is only 6.29% for a 32-kB cache. We also evaluate the induced performance degradationunder various fault densities using the CPU2000 and CPU2006 benchmark programs. The results show that for a 32-kB cache design, when the fault density is <;1%, only 0.31% performancedegradation is incurred. In addition, the scalability of the PDT cache is also evaluated. The results show that a smaller hardware overhead is required for a larger cache, and the performance degradation is independent of the cache associativity and can even be smaller for a larger cache under a given fault density.
VLSI16NXT08	**TITLE: An FPGA Architecture and CAD Flow Supporting Dynamically Controlled Power Gating** **ABSTRACT:** Leakage power is an important component of the total power consumption in field-programmable gatearrays (FPGAs) built using 90-nm and smaller technology nodes. Power gating was shown to be effective at reducing the leakage power. Previous techniques focus on turning OFF unused FPGAresources at configuration time; the benefit of this approach depends on resource utilization. In this paper, we present an FPGA architecture that enables dynamically controlled power gating, in whichFPGA resources can be selectively powered down at run-time. This could lead to significant overall energy savings for applications having modules with long idle times. We also present a CAD flow that can be used to map applications to the proposed architecture. We study the area and power tradeoffs by varying the different FPGA architecture parameters and power gating granularity. The proposedCAD flow is used to map a set of benchmark circuits that have multiple power-gated modules to the proposed architecture. Power savings of

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	up to 83% are achievable for these circuits. Finally, we study a control system of a robot that is used in endoscopy. Using the proposed architecture combined with clock gating results in up to 19% energy savings in this application.
VLSI16NXT09	**TITLE: An FPGA Implementation for Solving the Large Single-Source-Shortest-Path Problem** **ABSTRACT:** Single source shortest path (SSSP) is a fundamental problem in graph theory. However, the existing SSSP implementations on field-programmable gate arrays (FPGAs) are incapable of processing largegraphs by storing the graph and results in internal memories. In this brief, we propose a parallel FPGAimplementation to solve the SSSP problem, which is derived from a variant of the "eager" Dijkstra algorithm. In order to process a large graph problem, an extended systolic array priority queue called ExSAPQ is proposed to allow large-scale priority queue processing. The experimental results on the full United States road network show that our SSSP implementation on FPGA can achieve a speedup of 5× over the CPU implementation and the power consumption is only 1/4 of the latter.
VLSI16NXT10	**TITLE: Design for Testability of Sleep Convention Logic** **ABSTRACT:** Testability is a major concern in industry for today's complex system-on-chip design. Design-for-testability (DFT) techniques are essential for any logic style, including asynchronous logic styles in order to reduce the test cost. Sleep convention logic (SCL) is a new promising asynchronous logicstyle that is based on the more well-known asynchronous logic style NULL convention logic (NCL). In contrast to the NCL, there are currently no design for testability methodologies existing for the SCL. The aim of this paper is to analyze the various faults within SCL pipelines and propose a scan-based DFT methodology to make the SCL testable. The proposed DFT methodology is then validated through a number of experiments, showing that the methodology provides a high test coverage (>99%). The complete DFT methodology as well as the scan chain and scan cell design are presented.

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VLSI16NXT11	**TITLE: Code Compression for Embedded Systems Using Separated Dictionaries** ABSTRACT: Engineers must consider performance, power consumption, and cost when designing embedded digitalsystems; furthermore, memory is a key factor in such systems. Code compression is a technique usedin embedded systems to reduce the memory usage. BitMask-based code compression is a modified version of dictionary-based code compression. The basic purpose of BitMask is to record mismatched values and their positions to compress a greater number of instructions; it can be used exclusively or incorporated with the reference instructions to decode the codewords. In this paper, we applied a smallseparated dictionary, and variable mask numbers were used with the BitMask algorithm to reduce the codeword length of high-frequency instructions. In addition, a novel dictionary selection algorithm was proposed to increase the instruction match rates. The fully separated dictionary method was used to improve the performance of the decompression engine without affecting the compression ratio (CR) (the compressed code size divided by original code size). Based on the experimental results, the proposed method can achieve a 7.5% improvement in the CR with nearly no hardware overhead.
VLSI16NXT12	**TITLE: Efficient Dynamic Virtual Channel Organization and Architecture for NoC Systems** **ABSTRACT:** A growing number of processing cores on a chip require an efficient and scalable communication structure such as network on chip (NoC). The channel buffer organization of NoC uses virtual channels(VCs) to improve data flow and performance of the NoC system. Dynamically allocated multiqueues (DAMQs) are an effective mechanism to achieve VC flow control with maximum buffer utilization. In this model, VCs employ variable number of buffer slots depending on the traffic. Despite the performance merits of DAMQs, it has some limitations. We propose a new input-port microarchitecture to support ourefficient dynamic VC (EDVC) approach that is built on DAMQ buffers. To demonstrate the advantages of EDVC, we compare its microarchitecture with

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	that of the conventional dynamic VC (CDVC), which also employs link-list tables for buffer organization. In terms of hardware, EDVC input-port organizationconsumes on average 61% less power for application-specific integrated circuit design when compared with the CDVC input port. The saving is even better when compared with VC regulator methodology. An EDVC approach can improve NoC latency by 48%-50% and throughput by 100% on average as compared with the CDVC mechanism.
VLSI16NXT13	**TITLE: Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks** **ABSTRACT:** Soft errors pose a reliability threat to modern electronic circuits. This makes protection against softerrors a requirement for many applications. Communications and signal processing systems are no exceptions to this trend. For some applications, an interesting option is to use algorithmic-based faulttolerance (ABFT) techniques that try to exploit the algorithmic properties to detect and correct errors. Signal processing and communication applications are well suited for ABFT. One example is fast Fourier transforms (FFTs) that are a key building block in many systems. Several protection schemes have been proposed to detect and correct errors in FFTs. Among those, probably the use of theParseval or sum of squares check is the most widely known. In modern communication systems, it is increasingly common to find several blocks operating in parallel. Recently, a technique that exploits this fact to implement fault tolerance on parallel filters has been proposed. In this brief, this technique is first applied to protect FFTs. Then, two improved protection schemes that combine the use of errorcorrection codes and Parseval checks are proposed and evaluated. The results show that the proposed schemes can further reduce the implementation cost of protection.
VLSI16NXT14	**TITLE: Functional Test Generation for Hard-to-Reach States Using Path Constraint Solving** **ABSTRACT:** Test generation for hard-to-reach states is important in functional verification. In this paper, we present apath constraint solving-

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	based test generation method (PACOST) which operates in an abstraction-guided semiformal verification framework to cover hard-to-reach states. PACOST combines concrete simulation and symbolic simulation on the design under verification for path constraint extraction and mutation, and uses a sequential path constraint extractor to generate a set of valid input vectors for exploring different simulation paths with different next states. It then works on a target state-oriented abstract model to select the next state with the smallest abstract distance. In addition, the value of register variables in control logic can be controlled by analyzing the data dependence between variables, which helps the simulation converge to the target states. Experimental results show that PACOST can generate shorter traces reaching hard-to-reach states, in comparison with previous abstraction-guided semiformal methods.
VLSI16NXT15	**TITLE: High-Performance Deadlock-Free ID Assignment for Advanced Interconnect Protocols** **ABSTRACT:** In a modern system-on-chip design, hundreds of cores and intellectual properties can be integrated into a single chip. To be suitable for high-performance interconnects, designers increasingly adoptadvanced interconnect protocols that support novel mechanisms of parallel accessing, including outstanding transactions and out-of-order completion of transactions. To implement those novel mechanisms, a master tags an ID to each transaction to decide in-order or out-of-order properties. However, these advanced protocols may lead to transaction deadlocks that do not occur in traditionalprotocols. To prevent the deadlock problem, current solutions stall suspicious transactions and in certain cases, many such stalls can incur serious performance penalty. In this brief, we propose a novel ID assignment mechanism that guarantees the issued transactions to be deadlock-free and results in significant reduction in the number of transaction stalls issued by masters. Our experimental results show encouraging performance improvements compared with previous works with little hardware and power overheads.

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VLSI16NXT16	**TITLE: High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels** **ABSTRACT:** In this paper, we present a carry skip adder (CSKA) structure that has a higher speed yet lower energyconsumption compared with the conventional one. The speed enhancement is achieved by applying concatenation and incrementation schemes to improve the efficiency of the conventional CSKA (Conv-CSKA) structure. In addition, instead of utilizing multiplexer logic, the proposed structure makes use of AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates for the skip logic. The structure may be realized with both fixed stage size and variable stage size styles, wherein the latter further improves the speed and energy parameters of the adder. Finally, a hybrid variable latency extension of the proposed structure, which lowers the power consumption without considerably impacting the speed, is presented. This extension utilizes a modified parallel structure for increasing the slack time, and hence, enabling further voltage reduction. The proposed structures are assessed by comparing their speed, power, and energy parameters with those of other adders using a 45-nm static CMOS technology for awide range of supply voltages. The results that are obtained using HSPICE simulations reveal, on average, 44% and 38% improvements in the delay and energy, respectively, compared with those of the Conv-CSKA. In addition, the power-delay product was the lowest among the structures considered in this paper, while its energy-delay product was almost the same as that of the Kogge-Stone parallel prefix adder with considerably smaller area and power consumption. Simulations on the proposed hybrid variable latency CSKA reveal reduction in the power consumption compared with the latest works in this field while having a reasonably high speed.
VLSI16NXT17	**TITLE: In-Field Test for Permanent Faults in FIFO Buffers of NoC Routers** **ABSTRACT:** This brief proposes an on-line transparent test technique for detection of latent hard faults which develop in first-input first-output buffers of routers during field operation of NoC. The technique involves repeating tests periodically to prevent accumulation of faults. A prototype

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	implementation of the proposed test algorithm has been integrated into the router-channel interface and on-line test has been performed with synthetic self-similar data traffic. The performance of the NoC after addition of the testcircuit has been investigated in terms of throughput while the area overhead has been studied by synthesizing the test hardware. In addition, an on-line test technique for the routing logic has been proposed which considers utilizing the header flits of the data traffic movement in transporting the testpatterns.
VLSI16NXT18	**TITLE: Low-Cost High-Performance VLSI Architecture for Montgomery Modular Multiplication** **ABSTRACT:** This paper proposes a simple and efficient Montgomery multiplication algorithm such that the low-costand high-performance Montgomery modular multiplier can be implemented accordingly. The proposed multiplier receives and outputs the data with binary representation and uses only one-level carry-save adder (CSA) to avoid the carry propagation at each addition operation. This CSA is also used to perform operand precomputation and format conversion from the carry-save format to the binary representation, leading to a low hardware cost and short critical path delay at the expense of extra clock cycles for completing one modular multiplication. To overcome the weakness, a configurable CSA (CCSA), which could be one full-adder or two serial half-adders, is proposed to reduce the extra clock cycles for operand precomputation and format conversion by half. In addition, a mechanism that can detect and skip the unnecessary carry-save addition operations in the one-level CCSA architecturewhile maintaining the short critical path delay is developed. As a result, the extra clock cycles for operand precomputation and format conversion can be hidden and high throughput can be obtained. Experimental results show that the proposed Montgomery modular multiplier can achieve higherperformance and significant area-time product improvement when compared with previous designs.

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VLSI16NXT19	**TITLE: Low-Cost Multiple Bit Upset Correction in SRAM-Based FPGA Configuration Frames** **ABSTRACT:** Radiation-induced multiple bit upsets (MBUs) are a major reliability concern in nanoscale technology nodes. Occurrence of such errors in the configuration frames of a field-programmable gate array (FPGA) device permanently affects the functionality of the mapped design. Periodic configurationscrubbing combined with a low-cost error correction scheme is an efficient approach to avoid such a permanent effect. Existing techniques employ error correction codes with considerably high overhead to mitigate MBUs in configuration frames. In this paper, we present a low-cost error-detection code to detect MBUs in configuration frames as well as a generic scrubbing scheme to reconstruct the erroneous configuration frame based on the concept of erasure codes. The proposed scheme does not require any modification to the FPGA architecture. Implementation of the proposed scheme on a Xilinx Virtex-6 FPGA device shows that the proposed scheme can detect 100% of MBUs in the configurationframes with only 3.3% resource occupation, while the recovery time is comparable with the previous schemes.

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VLSI16NXT20	**TITLE: LUT Optimization for Distributed Arithmetic-Based Block Least Mean Square Adaptive Filter** **ABSTRACT:** In this paper, we analyze the contents of lookup tables (LUTs) of distributed arithmetic (DA)- basedblock least mean square (BLMS) adaptive filter (ADF) and based on that we propose intra-iteration LUTsharing to reduce its hardware resources, energy consumption, and iteration period. The proposed LUToptimization scheme offers a saving of 60% LUT content for block size 8 and still higher saving for larger block sizes over the conventional design approach. We also present here the design of a register-based LUT matrix for maximal sharing of LUT contents and full-parallel LUT-update operation.Based on the proposed design approach, we have derived a DA-based architecture for the BLMS ADF, which is scalable for larger block sizes as well as higher filter lengths. We find that the hardware complexity of the proposed structure increases less than proportionately with input block size and filterlength. It offers a saving of 60% LUT-update per output and 59% LUT access per output over the recently proposed DA-based BLMS ADF structure for block size 8 and filter length 64. Besides, the proposed structure involves nearly 30% saving in the iteration period over the other for 16-bit coefficient word length. Application specific integrated circuit (ASIC) synthesis result shows that the proposed structure for block size 8 offers a saving of 48% area-delay product (ADP) and 53% energy per sample (EPS) over the existing DA-based BLMS ADF structure on average for different filter lengths, and offers 30% higher sampling rate due to its shorter iteration period. Compared with the existing DA-based LMS ADF structure, the proposed structure involves 68% less ADP and $1.6 times $ less EPS.
VLSI16NXT21	**TITLE: Sign-Magnitude Encoding for Efficient VLSI Realization of Decimal Multiplication** **ABSTRACT:** Decimal X x Y multiplication is a complex operation, where partial products (IPPs) intermediate are commonly selected from a set of precomputed radix-10 X multiples. Some works require only [0, 5] x X via recoding digits of Y to

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	one-hot representation of signed digits in [-5, 5]. This reduces the selection logic at the cost of one extra IPP. Two's complement signed-digit (TCSD) encoding is often used to represent IPPs, where dynamic negation (via one xor per bit of X multiples) is required for the recoded digits of Y in [-5, -1]. In this paper, despite generation of 17 IPPs, for 16-digit operands, we manage to start the partial product reduction (PPR) with 16 IPPs that enhance the VLSI regularity. Moreover, we save 75% of negating xors via representing precomputed multiples by sign-magnitude signed-digit (SMSD) encoding. For the first-level PPR, we devise an efficient adder, with two SMSD input numbers, whose sum is represented with TCSD encoding. Thereafter, multilevel TCSD 2:1 reduction leads to two TCSD accumulated partial products, which collectively undergo a special early initiated conversion scheme to get at the final binary-coded decimal product. As such, a VLSI implementation of 16 x 16-digit parallel decimal multiplier is synthesized, where evaluations show some performance improvement over previous relevant designs.
VLSI16NXT22	**TITLE: Hybrid Hardware/Software Floating-Point Implementations for Optimized Area and Throughput Tradeoffs** **ABSTRACT:** Hybrid floating-point (FP) implementations improve software FP performance without incurring the area overhead of full hardware FP units. The proposed implementations are synthesized in 65-nm CMOS and integrated into small fixed-point processors with a RISC-like architecture. Unsigned, shift carry, and leading zero detection (USL) support is added to a processor to augment an existing instruction set architecture and increase FP throughput with little area overhead. The hybrid implementations with USL support increase software FP throughput per core by 2.18x for addition/subtraction, 1.29x for multiplication, 3.07-4.05x for division, and 3.11-3.81x for square root, and use 90.7-94.6% less area than dedicated fused multiply-add (FMA) hardware. Hybrid implementations with custom FP-specific hardware increase throughput per core over a fixed-point software kernel by 3.69-7.28x for addition/subtraction, 1.22-2.03x for multiplication, 14.4x for division, and

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	31.9x for square root, and use 77.3-97.0% less area than dedicated FMA hardware. The circuit area and throughput are found for 38 multiply-add, 8 addition/subtraction, 6 multiplication, 45 division, and 45 square root designs. Thirty-three multiply-add implementations are presented, which improve throughput per core versus a fixed-point software implementation by 1.11-15.9x and use 38.2-95.3% less area than dedicated FMA hardware.
VLSI16NXT23	**TITLE: An Efficient Component for Designing Signed Reverse Converters for a Class of RNS Moduli Sets of Composite Form {2k,2P -1}** **ABSTRACT:** The application of residue number system (RNS) to digital signal processing lies in the ability to operate on signed numbers. However, the available RNS-to-binary (reverse) converters have been designed for unsigned numbers, which means that they do not produce signed outputs. Usually, some additional circuits are introduced at the output of the reverse converter to map the unsigned generated output into a signed number representation. This paper proposes a novel method to design reverse converters with signed output for a class of RNS moduli sets of composite form {2k,2P -1}. The structure of the modulo adder used in the last stage of the proposed converters is modified in order to reuse the internal circuits to produce the signed output. This adder component isespecially designed forachievingreverse converters with sign ed output, imposing very low area and delay overheads compared with unsigned converters. The proposed approach is applied to design reverse converters for different moduli sets and to implement application specific integrated circuits. Experimental results show that for a 4-moduli converter, the proposed design can outperform the traditional method to obtain signed outputs by improving the delay, chip-area, and energy consumption by up to 9%, 21%, and 35%, respectively.
VLSI16NXT24	**TITLE: Content Addressable Memory-Early Predict and Terminate Precharge of Match-Line** **ABSTRACT:** A novel content addressable memory (CAM) architecture with a simple but very effective precharge controller is presented. CAM is a hardware

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	search mechanism that precharges all its match lines (MLs) during the precharge phase, and a search is performed during the evaluate phase. With unique words stored in a CAM, all the MLs except the one, which matches with the search word have to be discharged for every search cycle. The MLs that mismatch will anyway drain the charge during the evaluation phase, here, those mismatching MLs are predicted early during the precharge phase to terminate the full precharging of such lines. This promises CAM with reduced power as well as improved search speed.
VLSI16NXT25	**TITLE: Scalable Approach for Power Droop Reduction During Scan-Based Logic BIST** **ABSTRACT:** The generation of significant power droop (PD) during at-speed test performed by Logic Built-In Self Test (LBIST) is a serious concern for modern ICs. In fact, the PD originated during test may delay signal transitions of the circuit under test (CUT): an effect that may be erroneously recognized as delay faults, with consequent erroneous generation of test fails and increase in yield loss. In this paper, we propose a novel scalable approach to reduce the PD during at-speed test of sequential circuits with scan-based LBIST using the launch-on-capture scheme. This is achieved by reducing the activity factor of the CUT, by proper modification of the test vectors generated by the LBIST of sequential ICs. Our scalable solution allows us to reduce PD to a value similar to that occurring during the CUT in field operation, without increasing the number of test vectors required to achieve a target fault coverage (FC).
VLSI16NXT26	**TITLE: Efficient Designs of Multiported Memory on FPGA** **ABSTRACT:** The utilization of block RAMs (BRAMs) is a critical performance factor for multiported memory designs on field-programmable gate arrays (FPGAs). Not only does the excessive demand on BRAMs block the usage of BRAMs from other parts of a design, but the complex routing between BRAMs and logic also limits the operating frequency. This paper first introduces a brand new perspective and a more efficient way of using a conventional two reads one write (2R1W) memory as a 2R1W/4R memory. By exploiting the 2R1W/4R as the

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	building block, this paper introduces a hierarchical design of 4R1Wmemory that requires 25% fewer BRAMs than the previous approach of duplicating the 2R1W module. Memories with more read/write ports can be extended from the proposed 2R1W/4R memory and the hierarchical 4R1W memory. Compared with previous xor-based and live value table-based approaches, the proposed designs can, respectively, reduce up to 53% and 69% of BRAM usage for 4R2W memory designs with 8K-depth. For complex multiported designs, the proposed BRAM-efficient approaches can achieve higher clock frequencies by alleviating the complex routing in an FPGA. For 4R3W memory with 8K-depth, the proposed design can save 53% of BRAMs and enhance the operating frequency by 20%.
VLSI16NXT27	**TITLE: OptiFEX: A Framework for Exploring Area-Efficient Floating Point Expressions on FPGAs With Optimized Exponent/Mantissa Widths** **ABSTRACT:** Field-programmable gate arrays (FPGAs) could outperform microprocessors on floating point computations due to massive parallelism, freedom on the selection of exponent/mantissa width, and utilization of simplified adders and multipliers. However, optimized use of resources and accuracy of the final implemented expression are two important issues in the implementation of floating point arithmetic expressions on FPGAs. High-level optimizations such as changing the form of floating point initial expression by arithmetic rules or deciding on the exponent and mantissa widths have significant effects on the resource usage, accuracy, and efficiency of the final implementation. In this paper, we introduce an optimization framework called OptiFEX, which enables designers to optimize an initial floating point expression in terms of the resource usage and the exponent and mantissa widths based on: 1) input intervals; 2) the smallest presentable number in the implementation; and 3) the maximum permitted error interval provided by the designer. First, we come up with some techniques to generate equivalent expressions for the initial expression, and we make use of some heuristics to speed up the process of equivalent expressions' generation. We

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	also propose a method to estimate the mantissa width. Finally, we introduce an algorithm to choose the best expressions in terms of the resource usage based on the estimated mantissa and exponent widths.
VLSI16NXT28	**TITLE: A Fault Tolerance Technique for Combinational Circuits Based on Selective-Transistor Redundancy** **ABSTRACT:** With fabrication technology reaching nano levels, systems are becoming more prone to manufacturing defects with higher susceptibility to soft errors. This paper is focused on designing combinational circuits for soft error tolerance with minimal area overhead. The idea is based on analyzing random pattern testability of faults in a circuit and protecting sensitive transistors, whose soft error detection probability is relatively high, until desired circuit reliability is achieved or a given area overhead constraint is met. Transistors are protected based on duplicating and sizing a subset of transistors necessary for providing the protection. In addition to that, a novel gate-level reliability evaluation technique is proposed that provides similar results to reliability evaluation at the transistor level (using SPICE) with the orders of magnitude reduction in CPU time. LGSynth'91 benchmark circuits are used to evaluate the proposed algorithm. Simulation results show that the proposed algorithm achieves better reliability than other transistor sizing-based techniques and the triple modular redundancy technique with significantly lower area overhead for 130-nm process technology at a ground level.
VLSI16NXT29	**Title: A 4096-Point Radix-4 Memory-Based FFT Using DSP Slices** **ABSTRACT:** This brief presents a novel 4096-point radix-4 memory-based fast Fourier transform (FFT). The proposed architecture follows a conflict-free strategy that only requires a total memory of size N and a few additional multiplexers. The control is also simple, as it is generated directly from the bits of a counter. Apart from the low complexity, the FFT has been implemented on a Virtex-5 field programmable gate array (FPGA) using DSP slices. The goal has

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	been to reduce the use of distributed logic, which is scarce in the target FPGA. With this purpose, most of the hardware has been implemented in DSP48E. As a result, the proposed FPGA is efficient in terms of hardware resources, as is shown by the experimental results.
VLSI16NXT30	**Title: Low-Power Split-Radix FFT Processors Using Radix-2 Butterfly Units** **ABSTRACT:** Split-radix fast Fourier transform (SRFFT) is an ideal candidate for the implementation of a low-power FFT processor, because it has the lowest number of arithmetic operations among all the FFT algorithms. In the design of such processors, an efficient addressing scheme for FFT data as well as twiddle factors is required. The signal flow graph of SRFFT is the same as radix-2 FFT, and therefore, the conventional address generation schemes of FFT data could also be applied to SRFFT. However, SRFFT has irregular locations of twiddle factors and forbids the application of radix-2 address generation methods. This brief presents shared-memory low-power SRFFT processor architecture. We show that SRFFT can be computed by using a modified radix-2 butterfly unit. The butterfly unit exploits the multiplier-gating technique to save dynamic power at the expense of using more hardware resources. In addition, two novel address generation algorithms for both the trivial and nontrivial twiddle factors are developed. Simulation results show that compared with the conventional radix-2 shared-memory implementations, the proposed design achieves over 20% lower power consumption when computing a 1024-point complex-valued transform.
VLSI16NXT31	**Title: A Cache-Assisted Scratchpad Memory for Multiple-Bit-Error Correction** **ABSTRACT:** Scratchpad memory (SPM) is widely used in modern embedded processors to overcome the limitations of cache memory. The high vulnerability of SPM to soft errors, however, limits its usage in safety-critical applications. This paper proposes an efficient fault-tolerant scheme, called cache-assisted duplicated SPM (CADS), to protect SPM against soft errors. The main aim of CADS is to utilize cache memory to provide a replica for SPM lines. Using cache memory, CADS is able to guarantee a full duplication of all SPM

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	lines. We also further enhance the proposed scheme by presenting buffered CADS (BCADS) that significantly improves the CADS energy efficiency. BCADS is compared with two well-known duplication schemes as well as single-error correction scheme. The comparison results reveal that: 1) BCADS imposes a 13.6% less energy-delay product (EDP) overhead than the duplication schemes and it does not require to modify the SPM manager and target application and 2) in comparison with the conventional single-error correction double-error detection (SEC-DED) scheme, BCADS provides a significantly higher error correction capability by correcting up to 4-b burst errors using a low-cost 4-b interleaved parity code. Moreover, the area overhead for error correction and the performance overhead of BCADS are negligible (less than 1%), whereas the area and performance overheads are 21.9% and 6.1% for SEC-DED, respectively. Furthermore, BCADS imposes about a 10.7% lower EDP overhead compared with the SEC-DED scheme.
VLSI16NXT32	**Title: Multiplierless Unity-Gain SDF FFTs** **ABSTRACT:** In this brief, we propose a novel approach to implement multiplier less unity-gain single-delay feedback fast Fourier transforms (FFTs). Previous methods achieve unity-gain FFTs by using either complex multipliers or nonunity-gain rotators with additional scaling compensation. Conversely, this brief proposes unity-gain FFTs without compensation circuits, even when using nonunity-gain rotators. This is achieved by a joint design of rotators, so that the entire FFT is scaled by a power of two, which is then shifted to unity. This reduces the amount of hardware resources of the FFT architecture, while having high accuracy in the calculations. The proposed approach can be applied to any FFT size, and various designs for different FFT sizes are presented.

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VLSI16NXT33	**Title: A Test Selection Procedure for Improving the Accuracy of Defect Diagnosis** **ABSTRACT:** Procedures that were described earlier increase the accuracy of defect diagnosis by ignoring small subsets of tests in order to produce smaller candidate fault sets. The premise behind these procedures is that most of the tests in a given test set are useful for defect diagnosis, and only small numbers of tests need to be ignored. This paper makes the new observation that it is possible to use small subsets of tests to obtain more accurate diagnosis results. This paper describes a procedure that starts from an empty test set, and adds tests one at a time. The test selected at every iteration is the one that results in the smallest candidate fault set. The addition of tests increases the number of candidate faults gradually. Experimental results for benchmark circuits demonstrate that the addition of tests provides more candidate fault sets with higher degrees of accuracy than the removal of tests. One of these candidate fault sets can be used for failure analysis.
VLSI16NXT34	**Title: Precharge-Free, Low-Power Content-Addressable Memory** **ABSTRACT:** Content-addressable memory (CAM) is the hardware for parallel lookup/search. The parallel search scheme promises a high-speed search operation but at the cost of high power consumption. Parallel NOR- and NAND-type match line (ML) CAMs are suitable for high-search-speed and low-power-consumption applications, respectively. The NOR-type ML CAM requires high power, and therefore, the reduction of its power consumption is the subject of many reported designs. Here, we report and explore the short-circuit (SC) current during the precharge phase of the NOR-type ML. Also proposed here is a novel precharge-free CAM. The proposed CAM is free of the drawbacks of the charge sharing in the NAND and the SC current in the NOR-type CAM. Post layout simulations performed with a 45-nm technology node revealed a significant reduction in the energy metric: 93% and 77% lesser than NOR- and NAND-type CAMs, respectively. The Monte Carlo simulation for 500 runs was

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	performed to ensure the robustness of the proposed precharge-free CAM.
VLSI16NXT35	**Title: Variable Latency Speculative Parallel Prefix Adders for Unsigned and Signed Operands** **ABSTRACT:** A variable latency adder (VLA) reduces average addition time by using speculation: the exact arithmetic function is replaced by an approximated one, that is faster and gives correct results most of the times. When speculation fails, an error detection and correction circuit gives the correct result in the following clock cycle. Previous papers investigate VLAs based on Kogge-Stone, Han-Carlson or carry select topologies, speculating that carry propagation involves only a few consecutive bits. In several applications using 2's complement representation, however, operands have a Gaussian distribution and a nontrivial portion of carry chains can be as long as the adder size. In this paper we propose five novel VLA architectures, based on Brent-Kung, Ladner-Fisher, Sklansky, Hybrid Han-Carlson, and Carry increment parallel-prefix topologies. Moreover, we present a new efficient error detection and correction technique, that makes proposed VLAs suitable for applications using 2's complement representation. In order to investigate VLAs performances, proposed architectures have been synthesized using the UMC 65 nm library, for operand lengths ranging from 32 to 128 bits. Obtained results show that proposed VLAs outperform previous speculative architectures and standard (non-speculative) adders when high-speed is required.
VLSI16NXT36	**Title: Design of Efficient BCD Adders in Quantum Dot Cellular Automata** **ABSTRACT:** Among the emerging technologies recently proposed as alternatives to the classic CMOS, Quantum-dot cellular automata (QCA) is one of the most promising solutions to design ultra low-power and very high speed digital circuits. Efficient QCA-based implementations have been demonstrated for several binary and decimal arithmetic circuits, but significant improvements are still possible if the logic gates inherently available within the QCA technology are smartly exploited. This brief proposes a new approach to design QCA-

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	based BCD adders. Exploiting innovative logic formulations and purpose designed QCA modules, computational speed significantly higher than existing counterparts are achieved without sacrificing either the occupied area or the cells count.
VLSI16NXT37	**Title: An Improved DCM-based Tunable True Random Number Generator for Xilinx FPGA** **ABSTRACT:** True Random Number Generators (TRNGs) play a very important role in modern cryptographic systems. Field Programmable Gate Arrays (FPGAs) form an ideal platform for hardware implementations of many of these security algorithms. In this paper we present a highly efficient and tunable TRNG based on the principle of Beat Frequency Detection (BFD), specifically for Xilinx FPGA based applications. The main advantages of the proposed TRNG are its on-the-fly tunability through Dynamic Partial Reconfiguration (DPR) to improve randomness qualities. We describe the mathematical model of the TRNG operations, and experimental results for the circuit implemented on a Xilinx Virtex-V FPGA. The proposed TRNG has low hardware footprint and in-built bias elimination capabilities. The random bit streams generated from it passes all tests in the NIST statistical test suite.
VLSI16NXT38	**TITLE: A FPGA-based Unscented Kalman Filter for System-On-Chip Applications** **ABSTRACT:** Demand for fast and accurate state estimation in embedded systems has been increasing lately, at least in part due to mobile robotics such as UAVs. The desire to maintain high performance but with compact form factors leads to implementation issues especially with more complex systems. A hardware based approach using Field Programmable Gate Arrays (FPGAs) may be able to alleviate these issues but tends to have a more complicated development process than traditional software-based approaches. In order to simplify development and promote portability between embedded applications, a hardware/software co-design of the Unscented Kalman Filter (UKF) is presented. An example implementation (N = 18) of the hardware IP core only is

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	presented using the Zynq-7000 XC7Z045 with synthesis, power and timing results for the 1, 2, 5, and 10 processing element (PE) cases.
VLSI16NXT39	**TITLE: Register-Less NULL Convention Logic** **ABSTRACT:** NULL convention logic (NCL) is a promising design paradigm for constructing low-power robust asynchronous circuits. The conventional NCL paradigm requires pipeline registers for separating two neigh boring logic blocks, and those registers can account for up to 35% of the overall power consumption of the NCL circuit. This brief presents the register-less NULL convention logic (RL-NCL) design paradigm, which achieves low power consumption by eliminating pipeline registers, simplifying the control circuit, and supporting fine-grain power gating to mitigate the leakage power of sleeping logic blocks. Compared with the conventional NCL counterpart, the RL-NCL implementation of an eight-bit five-stage pipelined Kogge-Stone adder can reduce power dissipation by 56.4-72.5% for the input data rate ranging from 10 MHz to 900MHz. Moreover, the RL-NCL implementation can reduce the transistor count of the adder by 49.5%.
VLSI16NXT40	**TITLE: An FPGA-Based Cloud System for Massive ECG Data Analysis** **ABSTRACT:** In this brief, we propose a stand-alone SOPC (System on a Programmable Chip) based cloud system to accelerate massive ECG data analysis. The proposed system tightly couples network IO handling hardware to data processing pipelines in a single FPGA, offloading both networking operations and ECG data analysis. In this system, we first propose a massive sessions optimized TCP/IP hardware stack using a macro pipeline architecture to accelerate network packet processing. Second, we propose a streaming architecture to accelerate ECG signal processing, including QRS detection, feature extraction and classification. We verify our design on XC6VLX550T FPGA using real ECG data. Compared to commercial servers, our system shows up to 38X improvement in performance and 142X improvement in energy efficiency.

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VLSI16NXT41	**TITLE: LFSR-Based Generation of Multicycle Tests** **ABSTRACT:** This paper describes a procedure for computing a multicycle test set whose scan-in states are compressed into seeds for an LFSR, and whose primary input vectors are held constant during the application of a multicycle test. The goal of computing multicycle tests is to provide test compaction that reduces both the test application time and the test data volume. To avoid sequential test generation, the procedure uses a single-cycle test set to guide the computation of multicycle tests. The procedure optimizes every multicycle test, and increases the number of faults it detects, by adjusting its seed, primary input vector, and number of functional clock cycles. Optimizing the seed instead of the scan-in state avoids the computation of scan-in states for which seeds do not exist. Experimental results for benchmark circuits are presented to demonstrate the effectiveness of the procedure.
VLSI16NXT42	**TITLE: Area-Delay Efficient Digit-Serial Multiplier Based on-Partitioning Scheme Combined With TMVP Block Recombination Approach** **ABSTRACT:** Shifted polynomial basis (SPB) and generalized polynomial basis (GPB) are two efficient bases of representation in binary extension fields, and are widely studied. In this paper, we use the GPB formulation to derive a new modified SPB (MSPB) representation for arbitrary irreducible trinomials and pent anomials. It is shown that the basis conversion from the MSPB to the SPB for trinomials is free of hardware cost. We have shown that multiplication based on SPB and MSPB representations can make use of To eplitz matrix-vector product (TMVP) formulation. The existing TMVP block recombination(TMVPBR) approach is used here to derive an efficient k-partitioning TMVPBR decomposition for digit-serial double basis multiplication that can achieve sub quadratic space complexity. From synthesis results, we have shown that the proposed multiplier has less area and less area-delay product compared with the

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	existing digit-serial multipliers. We also show that the proposed multiplier using k-partitioning TMVPBR decomposition can provide a better tradeoff between time and space complexities.
VLSI16NXT43	**TITLE: Early Selection of Critical Paths for Reliable NBTI Aging-Delay Monitoring** **ABSTRACT:** Aging effects in advanced technologies produce significant performance degradation as time progresses. In order to guarantee safe operation, aging-delay monitors can be inserted at the output nodes of critical paths (CPs) to allow predictive error detection. However, online monitoring of a large number of CPs that can exist in the state-of-art designs is not feasible. The conventional statistical selection of CPs requires knowledge of the coordinates of each gate in the corresponding layout of the circuit to account for spatial correlation between devices' process parameters. This paper presents a non spatial-correlation-dependent methodology to select the CPs for aging-delay monitoring for predictive error detection. Spatial correlation is bounded by a statistical approach maximizing CPs' coverage. The proposed early selection methodology is validated by comparing the obtained results with those obtained with the availability of spatial correlation information extracted from the circuit layout. The results clearly show that the set of CPs selected with the proposed early selection methodology is in good agreement with the one selected with the availability of layout information. Therefore, our proposed methodology is very attractive to be used in the early design stages, where detailed circuit layout is not available.

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VLSI16NXT44	**TITLE: A New Fast and Area-Efficient Adder-Based Sign Detector for RNS** **ABSTRACT:** The moduli set $\{2^n - 1, 2^n, 2^n + 1\}$ has been widely used in residue number system (RNS)-based computations. Its sign extraction problem, albeit fundamentally important in magnitude comparison and other difficult algorithms in RNS, has received considerably less attention than its scaling and reverse conversion problems. This brief presents a new algorithm for the design of a fast adder-based sign detector. The circuit is greatly simplified by shrinking the dynamic range to eliminate large modulo operations with the help of the new Chinese remainder theorem. Our synthesis results with the 65-nm CMOS standard cell library show that the proposed design outperforms all the existing adder-based sign detectors reported for this moduli set in area and speed for n ranges from 5 to 25 in the step of 5.
VLSI16NXT45	**TITLE: Bit-Interleaving-Enabled 8T SRAM With Shared Data-Aware Write and Reference-Based Sense Amplifier** **ABSTRACT:** This brief proposes the design of a low-voltage static random access memory (SRAM) for biomedical chip applications. The SRAM is designed using a standard 8T bit cell, featuring a shared data-aware write scheme and a differential reference-based sense amplifier. The proposed techniques make it possible for the 8T SRAM to use bit-interleaving architecture and address the half-select problem, achieving area efficiency and power reduction. A 96-kb 8T SRAM test chip is implemented in a 65-nm CMOS process to verify the proposed schemes, which operates functionality at a VDD_{min} of 0.36 V and has a power consumption of 5.1 µW.

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VLSI16NXT46	**TITLE: NR-DCSK: A Noise Reduction Differential Chaos Shift Keying System** **ABSTRACT:** One of the major drawbacks of the conventional differential chaos shift keying (DCSK) system is the addition of channel noise to both the reference signal and the data-bearing signal, which deteriorates its performance. In this brief, we propose a noise reduction DCSK system as a solution to reduce the noise variance present in the received signal in order to improve performance. For each transmitted bit, instead of generating β different chaotic samples to be used as a reference sequence, β/P chaotic samples are generated and then duplicated P times in the signal. At the receiver, P identical samples are averaged, and the resultant filtered signal is correlated to its time-delayed replica to recover the transmitted bit. This averaging operation of size P reduces the noise variance and enhances the performance of the system. Theoretical bit error rate expressions for additive white Gaussian noise and multipath fading channels are analytically studied and derived. Computer simulation results are compared to relevant theoretical findings to validate the accuracy of the proposed system and to demonstrate the performance improvement compared to the conventional DCSK, the improved DCSK, and the differential-phase-shift-keying systems.
VLSI16NXT47	**TITLE: Efficient WLS Design of IIR Digital Filters Using Partial Second-Order Factorization** **ABSTRACT:** In this brief, a novel algorithm is developed for the design of infinite-impulse-response digital filters in the weighted least-squares sense. To simplify the design problem, the Levy linearized function and the Sanathanan-Koerner iterative technique are utilized. In the proposed algorithm, a denominator polynomial is decomposed as a cascade of a few second-order factors (SOFs) and a higher order factor (HOF). They are sequentially updated in each iteration. When updating SOFs composed of poles that are tending to be outside the unit circle, necessary and sufficient stability conditions

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	are taken into account, while the HOF is optimized without any stability constraint. The number of SOFs can be automatically determined in the proposed design procedure, which is convenient for practical designs. Simulation results demonstrate that the proposed algorithm can attain a balance between computational efficiency and design accuracy.
VLSI16NXT48	**TITLE: Fault Diagnosis for Leakage and Blockage Defects in Flow-Based Microfluidic Biochips** **ABSTRACT:** Advances in flow-based micro fluidics now allow an efficient implementation of biochemistry on-a-chip for DNA sequencing, drug discovery, and point-of-care disease diagnosis. However, the adoption off low-based biochips is hampered by defects that frequently occur in chips fabricated using soft lithography techniques. Recently published work has shown how we can automate the testing of flow-based biochips; diagnosis methods are now needed to identify the flaws in the fabrication process and to facilitate the use of partially defective chips. Since disposable biochips are being targeted for a highly competitive and low-cost market segment, such diagnosis methods need to be inexpensive, quick, and effective. In this paper, we present the first approach for the automated diagnosis of leakage andblockage defects in flow-based microfluidic biochips. The proposed method targets the identification off ault types and their locations based on test outcomes. It reduces the number of possible fault sites significantly while identifying their exact locations. We use a graph representation of flow paths and a formulation based on hitting sets for the analysis of observed error syndromes. The diagnosis technique is evaluated on three fabricated biochips, and the localization of faults and their classification are achieved correctly in all cases.

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VLSI16NXT49	**TITLE: Parallelized Network-on-Chip-Reused Test Access Mechanism for Multiple Identical Cores** **ABSTRACT:** This paper proposes a new network-on-chip (NoC)-reused test access mechanism (TAM) for testing multiple identical cores. It can test multiple cores concurrently and identify faulty cores to derate the chip by excluding the core. In order to minimize the test time, the TAM utilizes the majority value of test response data. All of the cores can thereby be tested in parallel and test costs (in both test pins and test time) are exactly the same as those for a single core. The hardware overhead is minimized by reusing the No C infrastructures and transfer-counters are designed as a majority analyzer. The experimental results in this paper show that the proposed TAM can test multiple cores in the same time as a single core and with negligible hardware overhead.
VLSI16NXT50	**TITLE: VLSI implementation of bit serial architecture based multiplier in floating point arithmetic.** **ABSTRACT:** VLSI implementation of Neural network processing or digital signal processing based applications comprises large number of multiplication operations. A key design issue, therefore in such applications depends on efficient realization of multiplier block which involves trade-off between precision, dynamic range, area, speed and power consumption of the circuit. The study in this paper investigates performance of VLSI implementation of bit serial architecture based multiplier (Type III) in floating point arithmetic (IEEE 754 Single Precision format). Results of implementation of 32x32 bit multiplier on FPGA as well as on Backend VLSI Design tool indicate that bit serial architecture based multiplier design provides good trade-off in terms of area, speed, power and precision over array multiplier and other multipliers approach proposed since last decade. In other words, bit serial architecture based multiplier (Type III) approach may provide good multi-objective solution for VLSI circuits.

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